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5G Systems and Packaging Opportunities

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Abstract

5G systems are being developed to meet the ever increasing desire for additional data bandwidth in mobile devices. Two enabling technologies for these systems are millimeter-wave electronics and phased arrays. Phased arrays have traditionally been used on military radar and satellite systems. However, they provide the capability to direct communication antenna beams directly to users or groups of users. In fact, standards committees agree that all network elements (including base stations, Access Points, and User Equipment) will be equipped with directional steerable antennas and can direct their beams in specific directions. In other words, phased arrays will be deployed at a variety of points in the 5G system even down to user equipment such as mobile phones, tablets, and lap tops. However, the components and modules used in 5G systems come with their unique packaging challenges. Those challenges will be described and some solutions will be given. 5G systems alternatives will also be described based on several architectures that are available for phased arrays. The two main reasons they are a challenge to package will be described. Several alternative solutions including heterogeneous packaging and 3D integration are described.

Section I: Introduction

Global mobile data usage is projected to grow from 11.2 Petabytes per month in 2017 to 48.3 Petabytes per month by 2021 and the compound annual growth rate from 2016-2021 is expected to be 46%. Meeting this need requires a complete rethinking of mobile data access. For this reason, mobile system developers are working to deliver 5G solutions to serve a highly mobile and fully connected society. The vision is for a 1000X increase in mobile data capacity, connecting 7 billion people and 7 trillion devices, while saving energy and reducing down time [1]. However, these goals cannot be achieved without significant technical advancements in system design and electronic packaging.

Two enabling hardware technologies for 5G are phased arrays and millimeter-wave systems and components. Previously, phased arrays have been used for military applications such as fighter airplane radar and satellite communication systems. However, they are being used or planned for use in multiple systems including 5G. In fact, the European 5G Public Private Partnership says that “we assume backhaul and access links share the same air interface, and all network elements (including BS [Base Stations], APs [Access Points] and UEs [User Equipment]) are equipped with directional steerable antennas and can direct their beams in specific directions [2]. In other words, phased arrays will be deployed at a variety of points in the 5G system even down to user equipment such as mobile phones, tablets, and lap tops. However, the components and modules used in 5G systems come with their unique packaging challenges. Those challenges will be described and some solutions will be given. 5G systems alternatives will also be described based on several architectures that are available for phased arrays. Several alternative solutions including heterogeneous packaging and 3D integration are described.

Section II: Phased Array System Description and Packaging Challenges

Phased arrays can be constructed many different ways. One approach is an Active Electronically Scanned Array (AESA) which is a common method that uses transmit receive (T/R) modules at each antenna element in the array. The packaging of T/R modules is a challenge for three reasons.

First, the array lattice spacing is small for 5G arrays operating at microwave and millimeter-wave frequencies. For many array designs, the lattice spacing is fixed at approximately half a wavelength according to

$$Lattice\ Spacing = \frac{\lambda}{2} = \frac{c}{2f} \quad (1)$$

Where:
λ = wavelength
f = frequency of operation for the phased array
c = speed of light = 3 x10^8 m/s.

From (1), it can be seen that as frequency increases, the lattice spacing decreases. For instance, at 20GHz, the lattice spacing is approximately 5.4mm at 28GHz. Lattice spacing is important for certain system performance parameters and for several electronic packaging reasons. For instance, lattice spacing determines the maximum beam steering angle (also called the field of view) for the array system. Lattice spacing sets the packaging density in the array which impacts signal coupling between circuits, packaging resonances, thermal performance, and material choices, to name a few.

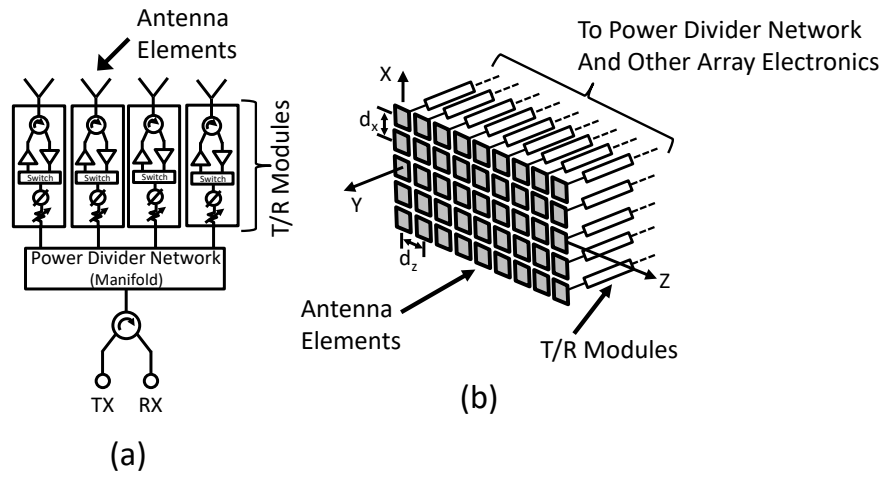

Fig. 1. Illustration of (a) an Active Electronically Scanned Array (AESA) subarray with four antenna elements each with a T/R module behind it, and (b) an array of 9 x 5 = 45 antenna elements.

This is illustrated in Fig. 1(a) which shows a four element subarray with T/R modules. This sub array can be assembled into a larger array as illustrated in Figure 1(b). Note that the spacing between antenna elements in the x-direction is shown as d_x and in the z-direction as d_z. This is the lattice spacing calculated using (1) for half wavelength spacing. The important point from a packaging perspective is that the size of the T/R module in the x and z-directions must fit within the lattice spacing which can be a significant packaging challenge at microwave and millimeter-wave frequencies.

The array lattice spacing places a limit on the maximum size of the T/R module in two dimensions with the max size in the third dimension constrained by factors such as fabrication capabilities, CTE mismatches, and mechanical stability. In that space, the T/R modules must be packaged along with the thermal management solution.

Second, the power density can be significant in T/R module because of the electronics used in the T/R module. In fact, for many 5G phased arrays, the thermal challenge is one of the factors that drives the packaging materials selected, cost of the array, and reliability. The thermal challenge can increase significantly for applications that require significant transmit signal power. In this case, high power amplifiers (HPA) may be required and will increase the thermal power density dissipated in the array. Consider an array at 28GHz (one of the 5G frequency bands) with an array lattice spacing of half wavelength ($d_x = d_y$ = 5.4mm) and 500mW of power dissipated at each element in the array. For a (12 x 12 elements) 144 element array, the overall array size is approximated as

$$L_x = Array\ Size\ in\ X \sim (n_x + 1)d_x \quad (2)$$

$$L_y = Array\ Size\ in\ y \sim (n_y + 1)d_y \quad (3)$$

Where:
n_x = number of elements in the x-direction
n_y = number of elements in the y-direction.

Note that factor of 1 in the equation approximates the half size antenna element that exists on either edge of the array. The size of the array using (2) and (3) is $L_x = L_y \sim$ 69.65mm. The power dissipated is 500mW x 144 elements = 72W. This results in a power density of 1.48 W/cm^2. The challenge that most low cost architectures for 5G phased arrays use panel type arrays with limited heat sinking capability.

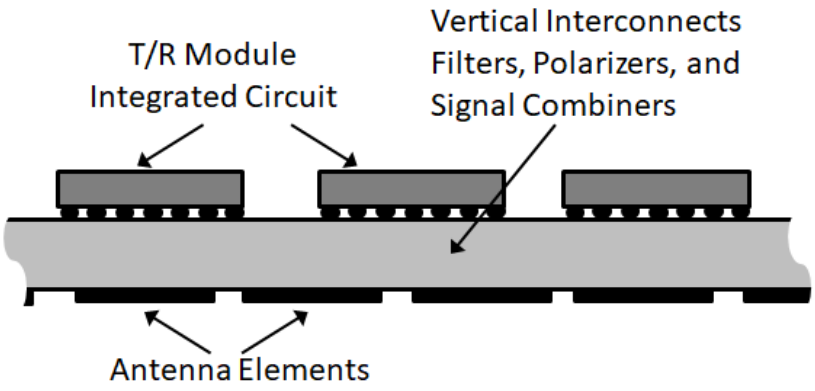

Fig. 2. Illustration of a panel array for 5G with integrated circuits on one side of the panel and antenna elements on the other side with passive circuits between them such as vertical interconnects, filters, polarizers, and signal combiners.

Third, the electrical interconnects can be a challenge due to the operating frequency. This often requires the use of millimeter-wave flip chips and vertical transitions. The challenge is that the array level interconnects must transition from the integrated circuits to the antenna elements. The antenna connections may require other circuits such as power dividers, circulators, filters, polarizers, or other duplexer circuit which are package between the integrated circuit and the antenna. Furthermore, the interconnect must transition from the layer in the array with the integrated circuit into the layer with the antenna element. This can be a significant challenge because even small discontinuities or impedance mismatches at 28GHz will spoil the performance of the antenna and integrated circuit. The electrical interconnect challenges from the integrated circuit to the antenna element are significant.

An alternative to AESAs is digital beam forming phased arrays. In this case, the integrated circuits include analog to digital converters and T/R module control circuitry. This eliminates the need for an analog power combiner (beam former) to combine the signals from each antenna element. However,

this method comes with its challenges too. One of the most significant is that a large number of high speed digital signals (differential in most cases) must be routed from each of the array antenna elements to other circuits such as field programmable gate arrays (FPGAs). The challenge is that the signal lines can operate at multiple Gb/s which means that transmission lines must be used to route this signals with minimal coupling between adjacent circuits. While digital beam forming has its advantages, there are also challenges [3] which can include increased heat dissipation in the integrated circuit further complicating the thermal challenge.

Section III: Packaging Solutions

There are several packaging approaches for 5G modules. One approach is to use ceramics such as high temperature co-fired ceramic (HTCC) alumina or low temperature co-fired ceramic (LTCC). One of the challenges with using ceramics is the signal losses that can occur. For HTCC alumina, for instance, the metal used in the buried layers is often a refractory metal such molybdenum (Mo) but the electrical conductivity of refractory metals is lower than for noble metals such as silver, gold, or copper. That said, if the electrical signal paths are kept short to minimize signal losses, HTCC may be a solutions for some systems. LTCC may be a more attractive solution for some 5G systems. It uses noble metals since it is processed at lower temperatures which noble metals can be processed. In addition, the dielectric loss of some LTCC materials is a bit lower than some alumina ceramics with further reduces the losses. One of the concerns with LTCC is the wide tolerance on the metal features in the finished substrates due to variability in the shrinkage during the firing process and flatness. Nevertheless, LTCC can still be attractive since it has higher thermal conductivity compared to some of the laminate solutions that are available. It can have thermal conductivities in the range of 2-4 W/mK. This is 5 to 20 times better thermal conductivity than most PCB materials. HTCC alumina has even better thermal conductivity at 17 to 25 W/mK which is about 5 to 10 times better than for LTCC. For these reasons, ceramics are one alternative for 5G phased array packaging but there are many tradeoffs to be made that require analysis and system benefit analysis.

For cost considerations and other reasons, laminate circuit boards are being considered as a solution. The attraction has increased significantly due to improved processing methods such as modified-semi-additive process (mSAP) [4]. It provides processing of fine line substrates along with a high degree of automation. As yields continue to improve for this process, it may become a dominate solution for 5G systems if the array thermal issues can be solved.

One of the challenges in 5G systems is the balance of cost, performance, and level of integration at the integrated circuit and packaging level. Specifically, silicon (Si) integrated circuit solutions provide high levels of integration such as analog circuits along with digital circuits while others provide lower noise figure and higher power density transistors such as gallium arsenide (GaAs) and indium phosphide (InP). An ideal solution for 5G may be the ability to integrate various integrated circuit technologies into a single solution. Therefore, heterogeneous integration is one possible solution. It is a transistor-scale integration processes to intimately combine compound semiconductor devices (such as GaAs, InP, GaN, and SiGe), as well as other materials and devices, with high-density silicon complementary metal-oxide-semiconductor (Si-CMOS) technology [5, 6]. The goal of this technology is to achieve performance levels at price points that are attractive for 5G and other applications. This approach includes some solutions that combine ceramic packaging with high density laminate which may be an approach to address the cost and thermal performance required for many 5G systems.

Section IV: Conclusions

5G and system architecture for phased array solutions are described. Transmit receive modules contained in phased arrays are also explained. It was shown that there are significant electronic packaging challenges for phased arrays due to lattice spacing requirements, frequency of operation, and thermal dissipation of the electronics. Some of the tradeoffs for material options are were given for several ceramics and laminates. Finally, electronic packaging technology options are described along with some of the advantages and challenges. This work provides information on 5G systems and some knowledge about the electronic packaging opportunities.

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