Design and Performance Of A High Density 3D Microwave Module

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Abstract

Microwave packaging involves the electrical interconnection, environmental protection and thermal management of active components such as MMICs, ASICs, and regulators as well as passive components like resistors, capacitors and substrates. The distinguishing feature between microwave modules and lower frequency modules is that the packaging dimensions are a significant fraction of a wavelength. This requires special care in the design of interconnects and substrate metalization. As packaging densities increase, concerns of coupling and high thermal density often drive the choice of materials and packaging configurations. This work describes the design and performance of a high density microwave module. The development of interconnects, thermal management and coupling reduction are described.

Introduction

System requirements of decreased volume, lower weight, and reduced cost have resulted in some significant improvements in microwave packages. One such improvements is the development of 3D high density microwave modules. These packages are characterized by stacked substrates, vertical transitions, and solderless interconnects. As a result, this type of module is capable of providing volume reductions of a factor of two, with significant cost and weight reductions. However, along with these benefits comes increased power density (up to 50W/in^2) at the module level. Also, issues of coupling, resonances, and maintaining ground continuity must be addressed. Furthermore, increased packaging density results in unique testability issues. First, the packaging concept will be presented showing materials choices and the module detail. Second, some of the key interconnects will be shown. Third, the test results of the individual, unstacked substrates will be shown. Finally, the measured performance of the full module will be presented.

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Packaging Concept

The application for this module is a transmit/receive (T/R) function. Four fully functional T/R modules are contained in the package. This includes power regulation, ASIC, amplitude and phase shifting MMICs, low noise MMICs, high power MMICs and various resistors and capacitors[1,2]. In fact, there are 24 MMIC flip chips, 4 flipped ASICs, 7 miscellaneous Si chips, 23 capacitors, and 12 resistors in a volume of approximately 3.05cm x 3.05cm x 0.102cm.

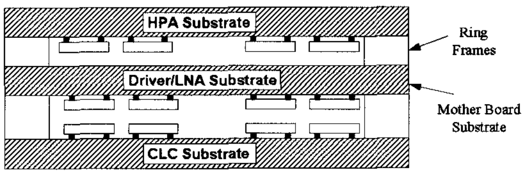

Figure 1. Stacked 3D module uses three substrates MMIC flip chips, and ring frames.

The general module concept is shown in Figure 1. It shows the stack of three substrates with two ring frames separating them. The ring frames serve to form a heat path, capture solderless interconnects, and provide physical spacing. The package can be laser welded or seam sealed for hermeticity.

The proper choice of materials is a critical step in the design cycle. It often determines the unit cost, performance and delivery schedule. An investigation into possible materials for the mother board substrate revealed aluminum nitride (AlN) was the best choice based upon the multilayer requirement to achieve the required density and the thermal path requirement. Table 1 shows a brief list of

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some of the material parameters for some typical mother board candidates for this module.

Material	TC (W/mK)	$\varepsilon_r/\tan\delta$	Multi-layer (?)
AlN	150	8.5/ 0.003	Y
LTCC	2	6-7/ 0.002	Y
Al_2O_3	25	9.8/ 0.0003	N*

Table 1. Possible materials choices for the stacked 3D module(* currently not available for microwave low loss applications).

Interconnects

The interconnects used in this module are vertical transitions and solderless interconnects[3]. The vertical transitions transfer energy vertically from the surface of the substrate to the backside or to a buried layer within the substrate. The solderless interconnects transfer energy from the surface of one substrate to the surface of another substrate or out from the module.

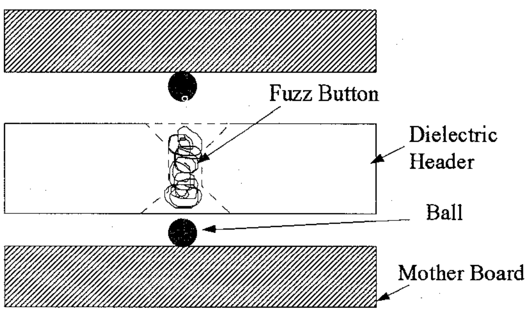

Figure 2. The mother boards are compressed to achieve electrical connection of the ball to fuzz.

Several vertical transitions and solderless interconnects have been developed and improved in our laboratories. One of the more recent interconnects is the ball to fuzz. The fuzz to ball interconnect is shown in Figure 2. A spherical ball made from brass or other material is attached to the motherboard while a fuzz button in a dielectric header is used to make electrical contact to the ball connection. This interconnect allows the fuzz button to be recessed within the dielectric header. Measured results show the return loss to be better than -18 dB up to 15 GHz. Proper design of the interconnect is required to achieve reliable connection as well as acceptable electrical performance.

Performance: Individual Substrates

As part of the experimental evaluation phase of the project, tests were conducted to determine the performance of each of the three substrates. Several substrates of each of the three types were fabricated and tested. In general, the test results and predicted performance agreed well. Figure 3 shows the measured output power for the Driver/LNA substrate. Note that it puts out about 1 Watt of power as expected even without test fixture losses removed. The test fixture has about 0.8-1.5 dB of loss.

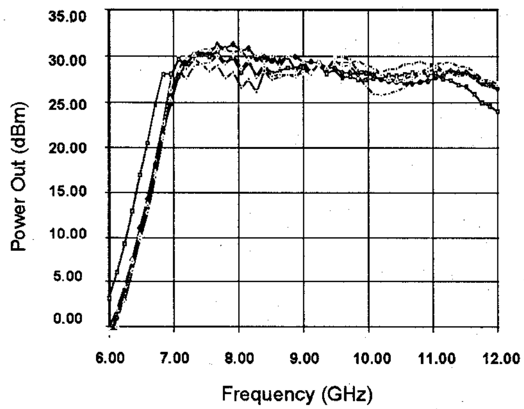

Figure 3. Measured performance of the Driver/LNA substrate with 10 dBm of input power (data not de-embedded).

The Driver/LNA substrate also has a receive portion. Figure 4 shows the measured receive gain. It is interesting to note that the measured gain for the mounted flip chip MMIC LNA is higher than the wafer level probe data. This effect is typical of flipped LNAs measured in our laboratories.

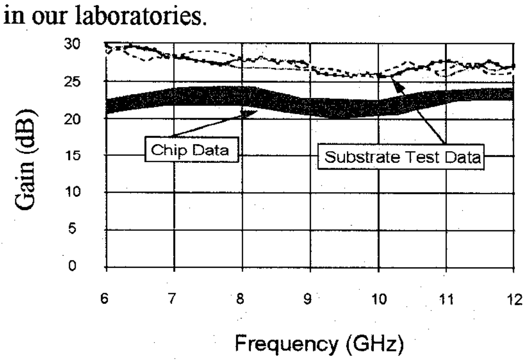

Figure 4. Measured receive gain of the Driver/LNA substrate.

The HPA substrate, which adds power gain to the module has a measured output power of 37.5-38 dBm. Figure 5 shows the typical measured performance of one channel on one of the substrates. Each of the four channels has two flipped HPA rated at 3.5-4 Watts output each. The expected output power is 38-39 dB ideal. Taking into account power combining inefficiencies and loss we expected 38 dBm. Our measurements agree with this prediction.

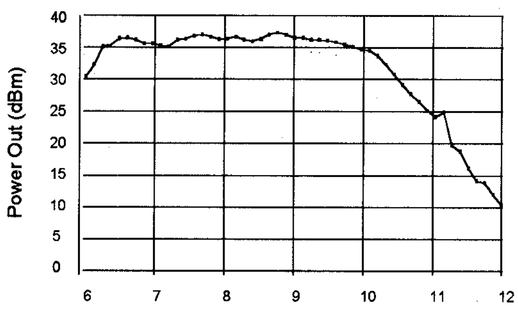

Figure 5. Measured output power of the HPA substrate (data de-embedded).

Performance: Full Stacked Module

The full module stack was also measured. As with the individual substrates, the tests were conducted using a fixture with a combination of solderless interconnects, CBCPW substrates, and Cascade Microtech GSG probes. Alignment of the individual substrates was a critical step in achieving module performance. This feature was achieved by proper design of the ring frames, and substrates to allow an automatic toleranced alignment while the stacking operation was performed.

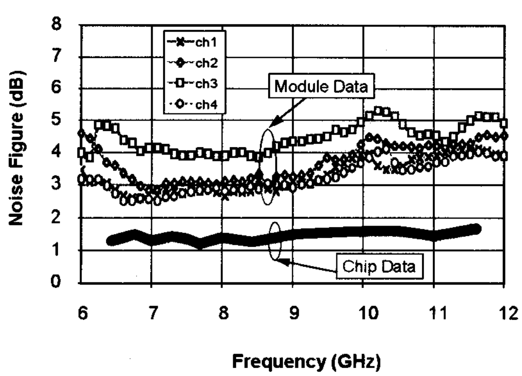

Figure 6. The module tests show low noise.

The measured noise figure is shown in figure 6. Note that the test data includes the loss of the test fixture so that the actual noise figure is about 0.8-1.5 dB less. In addition, since the LNA is contained on the middle substrate, the losses in the HPA substrate on the LNA path and the solderless interconnect add to the noise figure of the module. The associated module level gain is approximately 20 dB.

The MMICs used to achieve output power are flipped using thermal bumps over the FET source. This arrangement provides an optimal thermal path. Heat generated at the Gate-Drain area moves to the source and is taken out of the chip by the silver thermal bumps. Attachment of the MMIC chip to a high thermal conductivity substrate such as AlN provides a good thermal path to the heat sink. This arrangement provides an improved thermal path compared to conventional MMIC chips which must remove heat through the low thermal conductivity GaAs (~45 W/mK). In fact, modeling shows a 15 °C reduction in junction temperature for a flipped HPA MMIC using thermal bumps as compared to a conventional face up MMIC.

The module level output power was also measured and is shown in Figure 7. Note that the maximum output power is about 37 dBm. This is in agreement with our predicted result. Providing a good proper thermal path from the back of the AlN substrate to the test fixture during tests was a critical step in achieving the optimum output power.

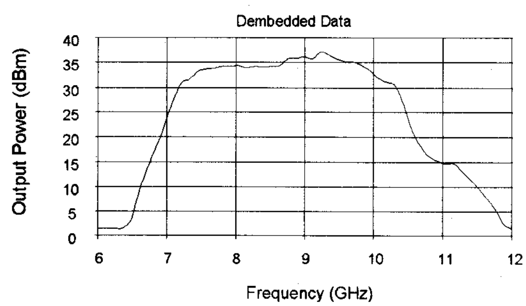

Figure 7. Module level output power tests show 37.5 dBm of output power. Use of improved MMIC chips is expected to result in several dB improvement in output power.

Conclusion

A unique module packaging approach is described along with some new interconnects. Test data is provided for the module demonstrating the ability of this innovative module technique to achieve simultaneous cost and size reductions while maintaining electrical performance. It is expected that stacked 3D module technology can be used in many new military applications as well as low cost commercial applications. This is due to the saving in substrate area and the reduction in overall volume and weight which are driving factors for military and commercial products.

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